UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,499	11/28/2003	Michael Cuylen	Q77791	7666

23373 7590 01/31/2008

SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
GANDHI, DIPAKKUMAR B	

ART UNIT	PAPER NUMBER
2117	

MAIL DATE	DELIVERY MODE
01/31/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Response to the Board of Patent Appeals and Interferences' order

As per the Board of Patent Appeals and Interferences' order on 01/15/2008, a full English translation of a foreign reference MASAO JP 59045738 is attached. The MASAO JP 59045738 reference was cited by the applicant in the Information Disclosure Statement filed on 8/24/2005 and it was considered by the examiner.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dipakkumar Gandhi
Patent Examiner

SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

PTO: 2007-1412
Japanese Published Unexamined (Kokai) Patent Publication No. 59-045738; Publication Date: March 14, 1984; Application No. 57-157230; Application Date: September 7, 1982; Int. Cl.^{3}: H04L 1/10 H03K 13/32; Inventor: Masao Gohara; Applicant: Fujitsu Ltd.; Japanese Title: Shokuretsu Densou Deeta Chekku Houshiki (Serial Transfer Data Checking System)

Specification

1. Title of Invention

Serial Transfer Data Checking System

2. Claim

A serial transfer data checking system, characterized in that at a device that carries out a data transfer serially at a bit, a circuit that makes a single addition or subtraction every time logic 1 is transferred per bit and a single subtraction or addition every time logic 0 is transferred per bit and a circuit that transfers information on the result of the addition and subtraction after the completion of the entire data transfer while the information is added to the end of the transfer data are provided on the transmitting side; a circuit that makes a single addition or subtraction every time logic 1 is received per bit and a single subtraction or addition every time logic 0 is received per bit and a circuit that compares information on the addition and subtraction result transferred from the transmitting side with information on the subtraction and addition result computed on the receiving side are provided on the receiving side; bit errors on a data transfer passage are detected based on the output of the comparator circuit.

3. Detailed Description of the Invention

(a) Field of Industrial Application

This invention pertains to a serial transfer data checking system that is capable of effectively detecting bit errors on a data transfer passage where a data transfer is serially carried out per bit.

(b) Problem to Be Solved by the Invention

As to a means for detection bit errors on a bit serial data transfer passage, a CRC system or a LRC system is usually used. At the CRC system, the detecting ratio of the bit errors is extremely high. However, the actualizing means is complicated. At the LRC system, the actualizing means is simple. However, errors in odd numbers of bits in the horizontal direction cannot be detected.

(c) Purpose of the Invention

The invention aims to detect errors in odd numbers of entire bits to be transferred at a certain level as well by an actualizing means as almost similarly to as in the LRC system.

(d) Scope of the Invention

In order to achieve the purpose, the invention is characterized in that at a device that carries out a data transfer serially at a bit, a circuit that makes a single addition or subtraction every time logic 1 is transferred at 1 bit and a single subtraction or addition every time logic 0 is transferred per bit and a circuit that transfers information on the

result of the addition and subtraction after the completion of the entire data transfer while the information is added to the end of the transfer data are provided on the transmitting side; a circuit that makes a single addition or subtraction every time logic 1 is received per bit and a single subtraction or addition every time logic 0 is received per bit and a circuit that compares information on the addition and subtraction result transferred from the transmitting side with information on the subtraction and addition result computed on the receiving side are provided on the receiving side; bit errors on a data transfer passage are detected based on the output of the comparator circuit.

(e) Working Example of the Invention

Fig.1 illustrates the components of a checker circuit as in the working example of the invention. The working example is as a bit serial transfer system that uses a shift register. The concept of the invention can be similarly adopted to other bit serial transfer systems as well.

In Fig.1, MPX refers to a Switcher circuit; UDCNT to an up-down counter; SFT1 to a shift register that converts parallel data into serial data; SFT2 to a shift register that converts serial data into parallel data; CMP to a comparator circuit.

An operation of the working example is described along Fig.1.

First, data to be transmitted are set at a fall timing for a transmission clock (ST) via MPX or directly to SFT1 when a parallel set enable (PS) signal is on. As the PS signal is off, the data set at the falling of the ST is shifted at a bit and transmitted to the receiving side. The output signal (SD) of SFT1 is also input to an UP/DOWN control terminal of UDCNT. As a checking starting command (DE) signal of the transmission

data is turned on, the difference in the transmitting numbers of "1" and "0" of the SD begins to be counted. Upon completion of the transmission of the entire data, the DE is turned off to stop the operation of UDCNT whereas a transmission completing signal (END) as not shown in the drawing is turned on. During the on state, MPX selects outputs CK0 to CKm of UDCNT. The outputs CK0 to CKm are set to SFT1 using the PS to be turned on again at a timing similarly to as in the END so that the PS is turned off. By this means, the outputs are shifted again to be transmitted to the receiving side. Upon completing of the transmission of the outputs CK0 to CKm, the ST stops. UDCNT is cleared when the END is off and when the PS is on.

On the receiving side, receiving data (RD) are input to SFT2, shifted at a rise timing of the ST, and received as parallel data. The RD is also input to UDCNT on the receiving side. The UDCNT operates as totally similarly to as on the transmitting side. After this, upon completing of the receiving the outputs from CK0 to CKm, the ST from the transmitting side stops. Thereby, outputs from the last bit of SFT2 to +(m+1) bit are held as check bits. By comparing the check bits held in SFT2 with the output of UDCNT using CMP, bit errors on a data transfer passage are detected. When the check bits do not match with the output of UDCNT, an error signal is output.

Above is a brief description of the operation. Fig.2 is a time chart illustrating a transmitting side operation at the time of the operation.

As described above, according to the invention, the difference in the numbers of bits at logic 1 and bits at logic 0 to be transmitted to the transmitting side is computed. The computation result is added to the data after the completion of the data transmission. The data are transmitted as a check code. On the receiving side also, the difference in the

numbers of bits at logic 1 and bits at logic 0 received as similarly to as on the transmitting side is computed. After the data receiving, a transmitted check code and the result computed on the receiving side are compared with each other. By these means, bit errors on the data transfer passage are detected.

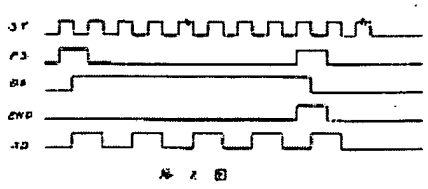
(f) Advantageous Result of the Invention

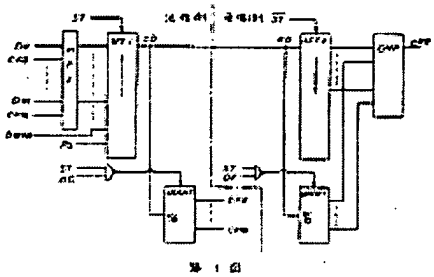
According to the invention, all errors except for errors that the number of bits with logic 1 erroneously substituted for logic 0 becomes equivalent to that of bits with logic 0 erroneously substituted for logic 1 are detected using a simple hardware structure, thereby obtaining a significant result.

4. Brief Description of the Drawings

Fig.1 illustrates a checker circuit structure as in the working example of the invention. Fig.2 illustrates an example of the time chart for a transmitting side operation.

In Fig.1, MPX refers to the switcher circuit; UDCNT to the up-down counter; SFT1 to the shift register that converts parallel data into serial data; SFT2 to the shift register that converts serial data into parallel data; and CMP to the comparator circuit.





U.S. Patent and Trademark Office
Translations Branch
12/19/06
Chisato Morohashi